Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory controller, comprising:

at least one bus interface, each bus interface being for connection to at least one respective device for receiving memory access requests;

a memory interface, for connection to a memory device over a memory bus;

a plurality of buffers; and

control logic, for placing received memory access requests into a queue of memory access requests,

wherein, in response to a received memory access request requiring multiple data bursts over the memory bus, data from each of said multiple data bursts is stored in a respective buffer of said plurality of buffers, and [[.]]

wherein, for a wrapping memory access request requiring multiple buffers, data required for a beginning and an end of the wrapping memory access request are stored in a single buffer of the plurality of buffers.

2. (Currently Amended) A memory controller as claimed in claim 1, wherein, when returning data to the respective device from which a memory access request requiring multiple data bursts over the memory bus was received, data is read out from a first part of ~~one of said buffers~~ the single buffer, then data is read out from at least one other of said buffers, then data is read out from a second part of ~~said one of said buffers~~ the single buffer.

3. (Original) A memory controller as claimed in claim 1, wherein said plurality of buffers is located in said memory interface.

Claim 4. (Canceled).

5. (Original) A memory controller as claimed in claim 1, wherein the control logic determines whether a received read access request is a wrapping request which requires multiple memory bursts, and, if so, the control logic allocates each of said memory bursts to a respective one of said buffers.

6. (Original) A memory controller as claimed in claim 1, wherein the memory controller is a SDRAM controller, and said memory interface is suitable for connection to a SDRAM memory device over said memory bus.

7. (Currently Amended) In a memory controller, comprising: at least one bus interface, each bus interface being for connection to at least one respective device for receiving memory access requests; a memory interface, for connection to a memory device over a memory bus; a plurality of buffers; and control logic, for placing received memory access requests into a queue of memory access requests, a method of retrieving data comprising:

in response to a received memory access request requiring multiple data bursts over the memory bus, storing data from each of said multiple data bursts in a respective buffer of said plurality of buffers, [[.]]

wherein, for a wrapping memory access request, data required for a beginning and an end of the wrapping memory access request are stored in a single buffer of the plurality of buffers.

8. (Currently Amended) A method as claimed in claim 7, further comprising when returning data to the respective device from which a memory access request requiring multiple data bursts over the memory bus was received, reading data out from a first part of ~~one of said buffers~~ single buffer, then reading data out from at least one other of said buffers, then reading data out from a second part of ~~said one of said buffers~~ the single buffer.

9. (Original) A method as claimed in claim 7, comprising storing said data from each of said multiple data bursts in a respective buffer in said memory interface.

10. (Original) A method as claimed in claim 7, comprising storing said data from each of said multiple data bursts in a respective buffer in said bus interface to which the respective device from which the memory access request was received.

11. (Original) A method as claimed in claim 7, comprising determining whether a received read access request is a wrapping request which requires multiple memory bursts, and, if so, allocating each of said memory bursts to a respective one of said buffers.

12. (Original) A method as claimed in claim 7, wherein the memory controller is a SDRAM controller, and said memory interface receives data from a SDRAM memory device over said memory bus in SDRAM bursts.

13. (Currently Amended) A programmable logic device, wherein the programmable logic device includes a memory controller, comprising:

at least one bus interface, each bus interface being for connection to at least one respective device formed within the programmable logic device for receiving memory access requests;

a memory interface, for connection to an external memory device over a memory bus;

a plurality of buffers; and

control logic, for placing received memory access requests into a queue of memory access requests,

wherein, in response to a received memory access request requiring multiple data bursts over the memory bus, data from each of said multiple data bursts is stored in a respective buffer of said plurality of buffers, and [[.]]

wherein, for a wrapping memory access request, data required for a beginning and an end of the wrapping memory access request are stored in a single buffer of the plurality of buffers.

14. (New) A memory controller as recited in claim 1, wherein each of the plurality of buffers includes a plurality of sub-buffers, data required for the beginning and the end of the wrapping memory access request being stored in separate sub-buffers of the single buffer.

15. (New) A memory controller as recited in claim 14, wherein the control logic is operable to record the value of a pointer indicating the sub-buffer from which data required for the end of the wrapping memory is to be retrieved from the single buffer.

16. (New) A method as recited in claim 7, wherein each of the plurality of buffers includes a plurality of sub-buffers, data required for the beginning and the end of the wrapping memory access request being stored in separate sub-buffers of the single buffer.

17. (New) A method as recited in claim 16, wherein the control logic is operable to record the value of a pointer indicating the sub-buffer from which data required for the end of the wrapping memory is to be retrieved from the single buffer.